XFTIIB: Online Track Processor for CDF RunIIB

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CDF Collaboration

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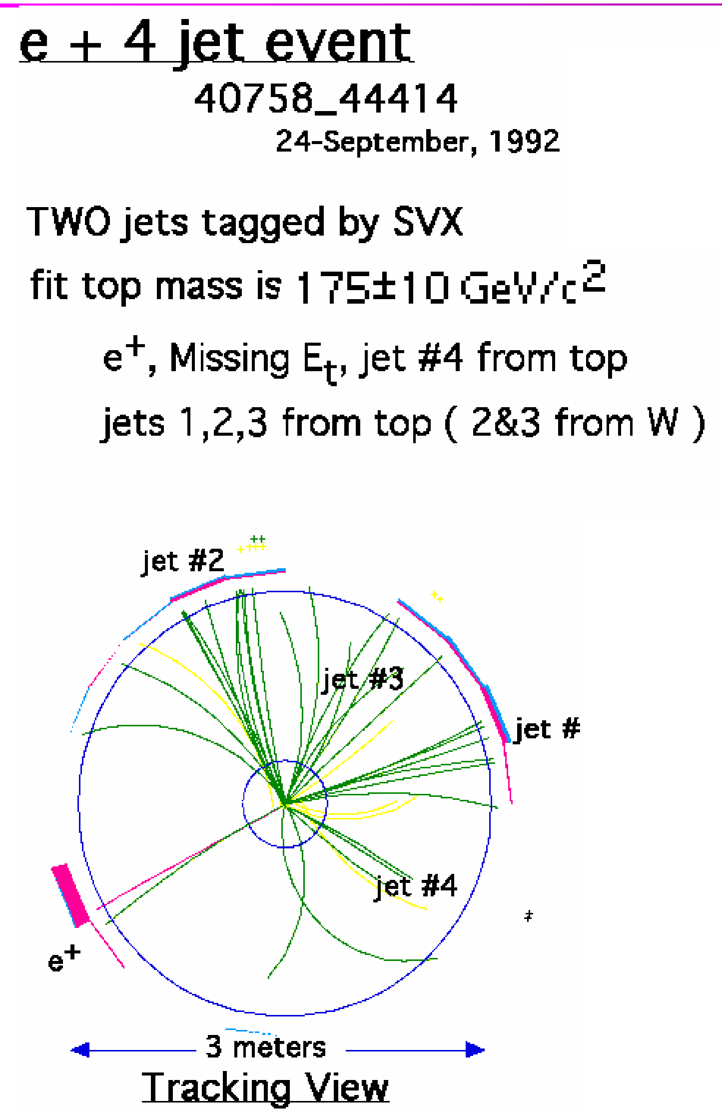
Lehman Review

XFT
Fast Tracking Trigger

- **Top** triggers require **High momentum** electron and muon candidates.
- Collision rate to Tape:
  - **7.5 MHz - to - 30 Hz**
- **Tracking** is a powerful tool to help reduce this rate and to extract the most interesting physics from large number of minimum bias events.



Tracking in the Level 1 Trigger

- Role of tracking
  - **Top, W/Z, Exotic Physics** triggers require **High momentum** electron and muon **Level 1 trigger** candidates
  - **Bottom Physics** require **low momentum** tracking at the

    Level 1 trigger
    - electrons
    - muons
    - hadronic tracks
- Trigger Electrons
  - Trigger track + EM cluster
- Trigger Muons
  - Trigger track + muon stub

- The tracking trigger needs to provide a track list in time for the Level 1 trigger decision
- The tracking trigger needs to find tracks every crossing, hence the name:

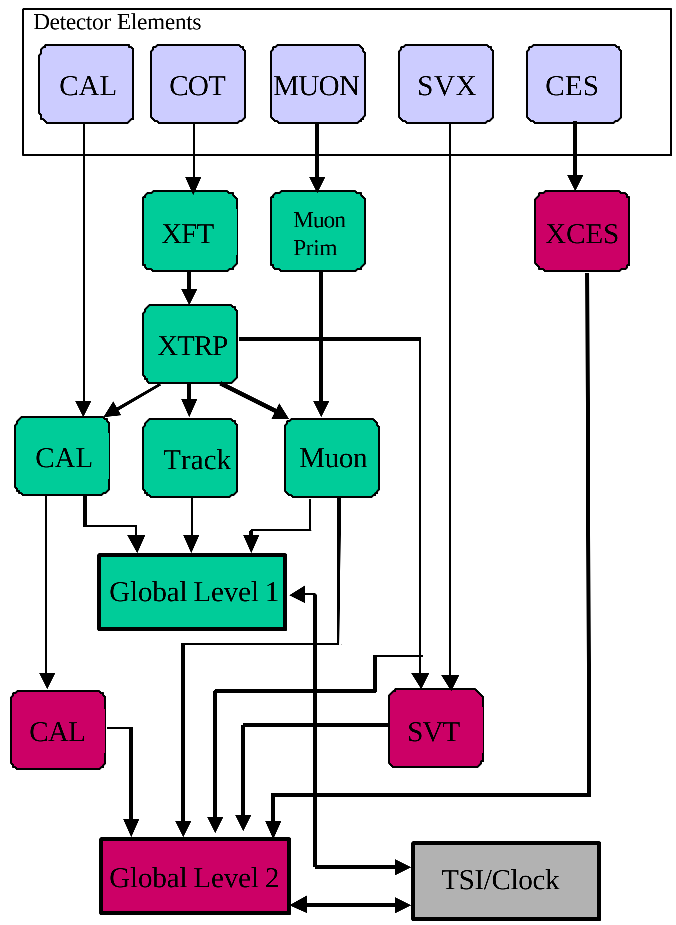
eXtremely Fast Tracker

XFT

XFT = eXtremely Fast Tracker

- Role of tracking
  - Top, W/Z, Exotic Physics triggers require High momentum electron and muon **Level 1 trigger** candidates
  - Bottom Physics require low momentum tracking at the

    Level 1 trigger
    - electrons
    - muons
    - hadronic tracks
- L1 Trigger Primitives
  - Electrons: XFT track + EM cluster
  - Muons: XFT track + muon stub
- L2 Trigger Tracks
  - XFT Track + Silicon Hits



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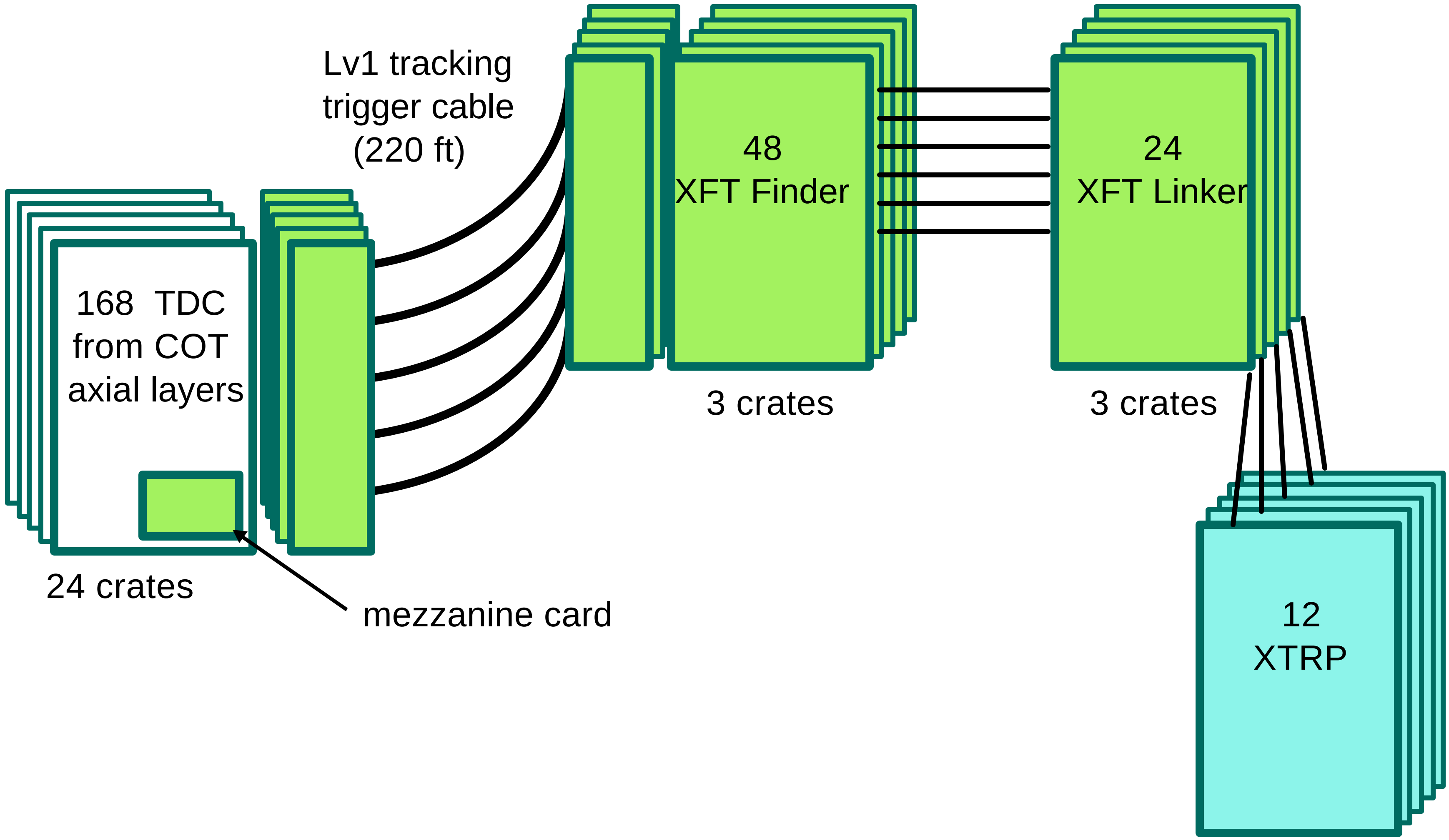
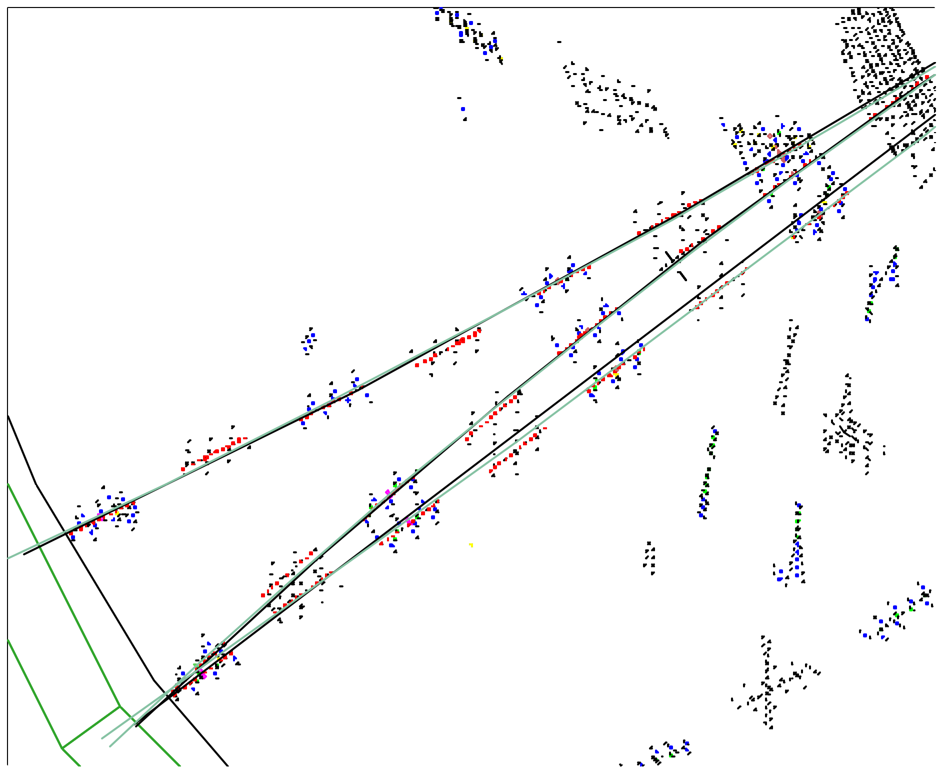
XFT Tracking Trigger



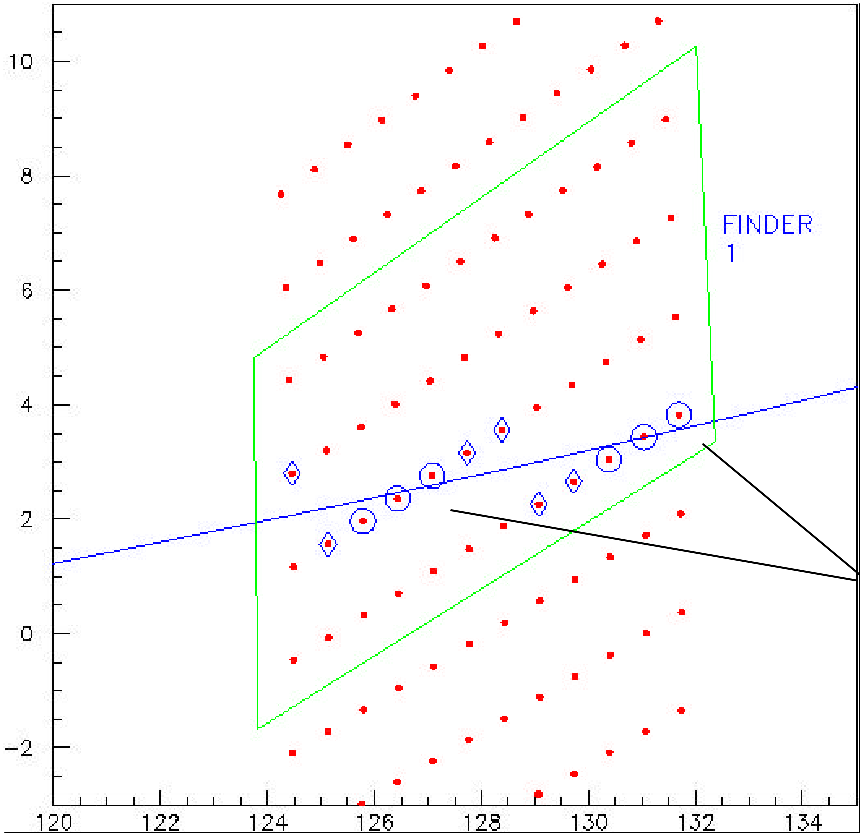
Outline of XFT Operation

- Hit Finding: Mezzanine Card
  - Hits are classified as prompt or delayed
- Segment Finding
  - In the axial layers, search for patterns of prompt/delayed hits consistent with High Pt tracks
  - Each segment found is assigned a pixel (phi, all layers) and possibly a slope (outer 2 axial layers only)
- Track Finding
  - Looking across 3 or 4 axial layers, search for patterns of segments consistent with Pt>1.5 GeV/c
  - Resultant Pt and Phi of all 1.5 GeV/c tracks sent on to XTRP
  - Maximum of 288 tracks reported



The Finder

Track segments are found by comparing hit patterns in a given layer to a list of valid patterns or "**masks**".



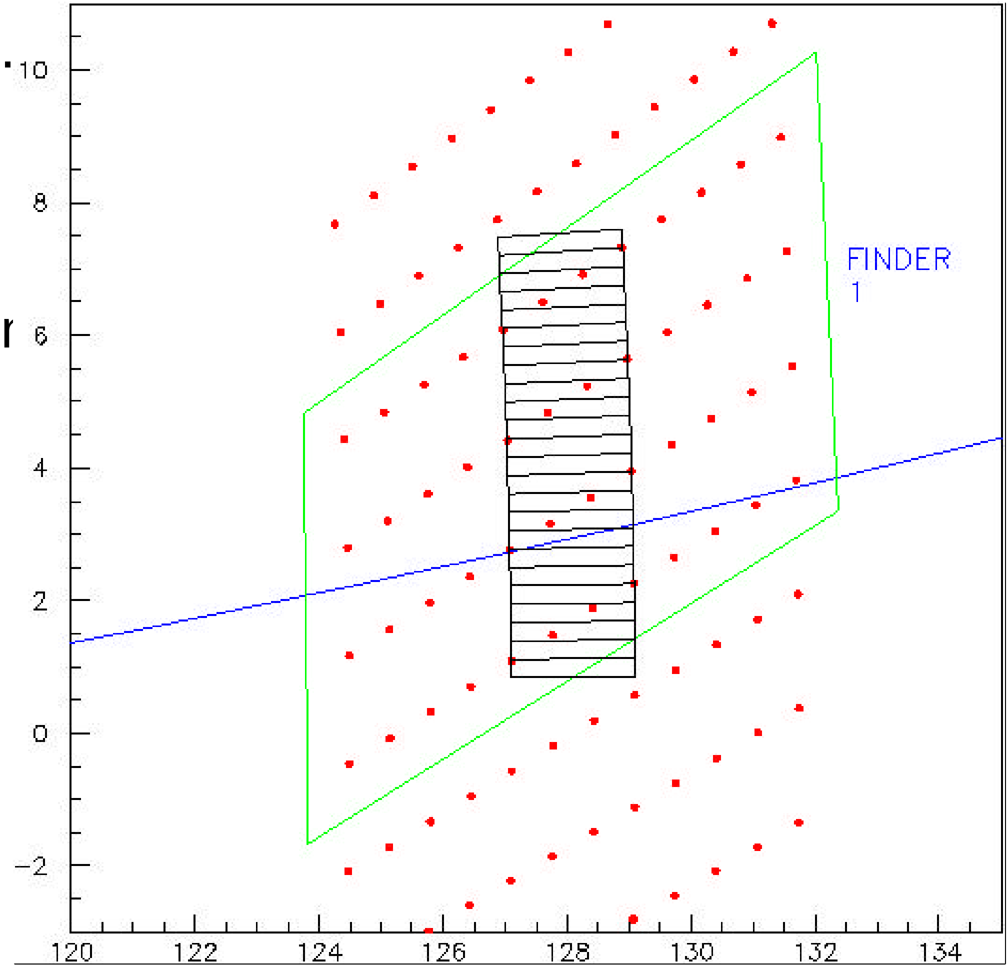
○ "Prompt" hit

◊ "Delayed" hit

Mask : A specific pattern of prompt and delayed hits on the 12 wires of an axial COT layer

Finder Output

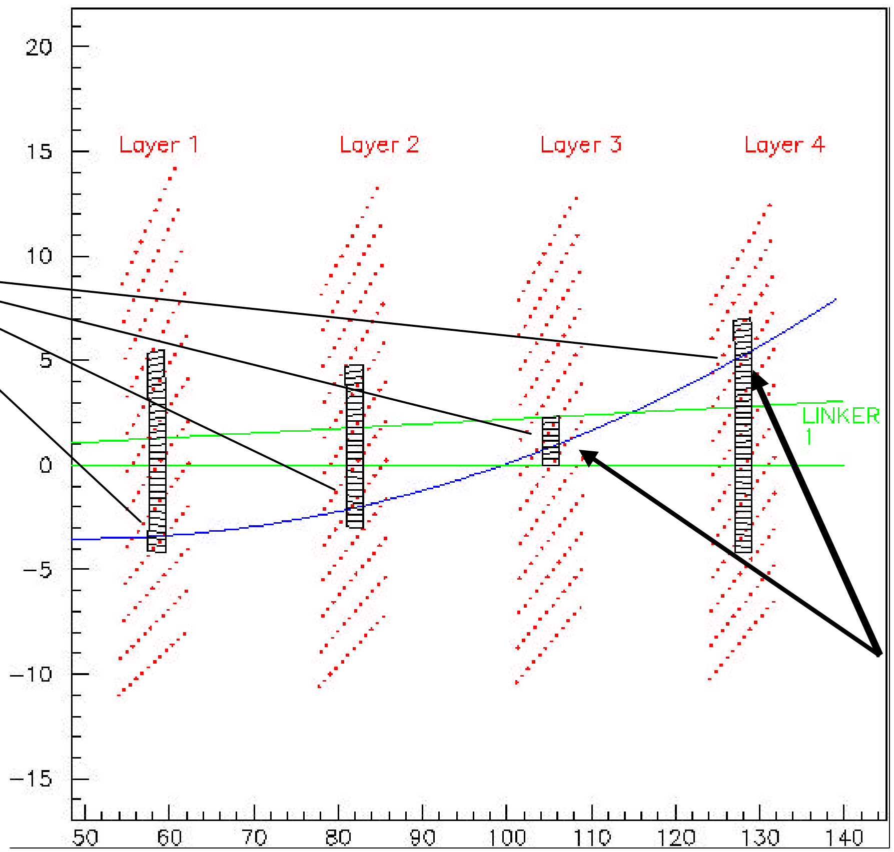
- In the **inner** two layers, each **mask** corresponds to 1 of 12 **pixel** positions in the middle of the layer.
- The **pixel** represents the **phi** position of the track.
- In the **outer** 2 layers, each **mask** corresponds to 1 of 6 **pixel** positior and 1 of 3 **slopes:** (low pt +, low pt -, high pt).
- When a **mask** is located, the corresponding **pixel** is turned on.



The Linker

Tracks are found by comparing fired **pixels** in all 4 layers to a list of valid **pixel** patterns or "**roads**".

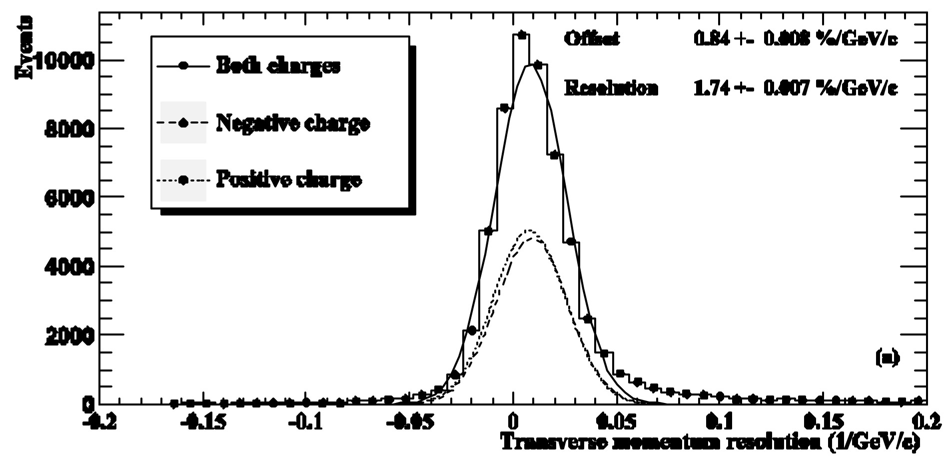
Pixels must match

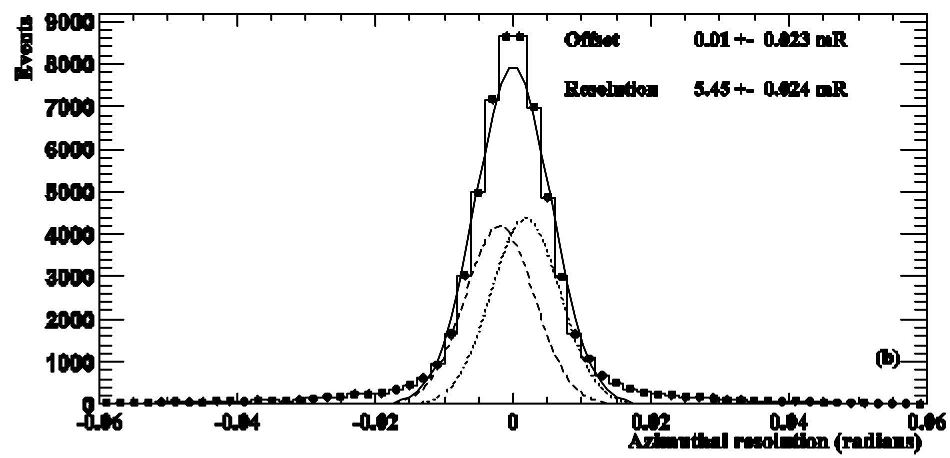


Slopes must match

XFT Performance in RunIIA

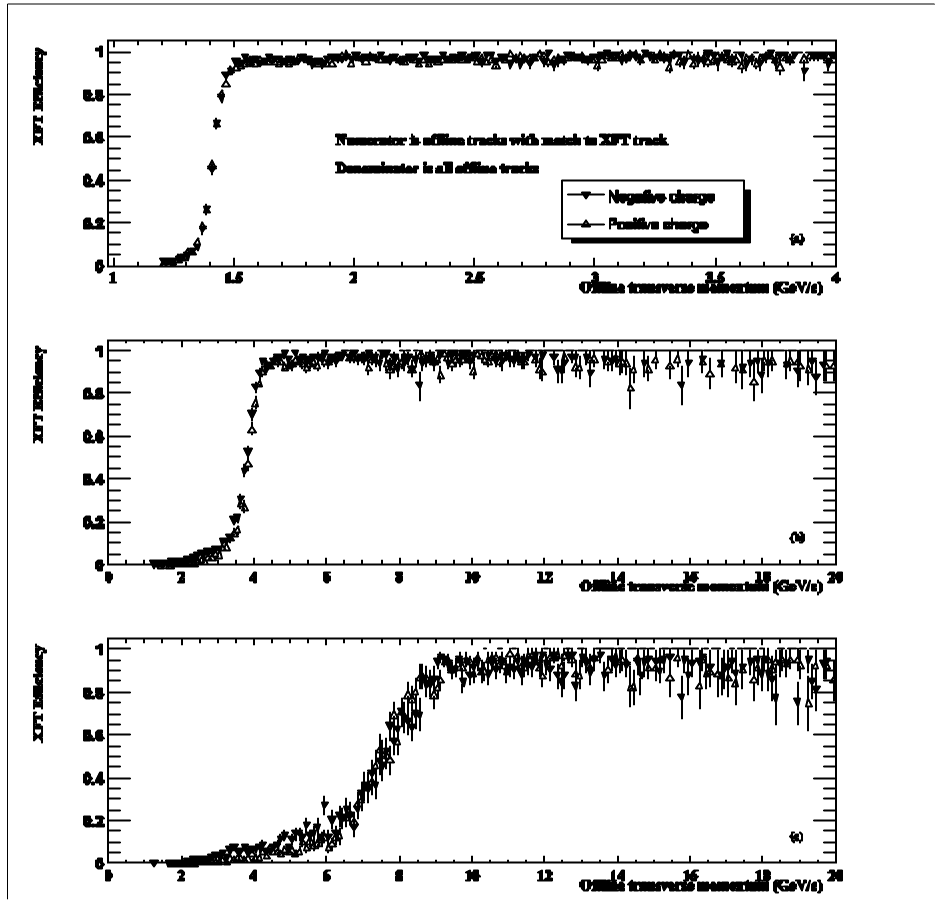
- The XFT was installed prior to the start of the Run II engineering run
- Performance of the XFT in RunIIa has been excellent
  - Present and working for all runs
  - Momentum resolution 1.74%/GeV/c
  - Phi Resolution < 6mRad
  - Efficiency > 95%
- Device can be run with a programmable number of allowed misses: 0,1,2,3.
  - Hit efficiency of COT lower than expected, so running with 2 allowed misses





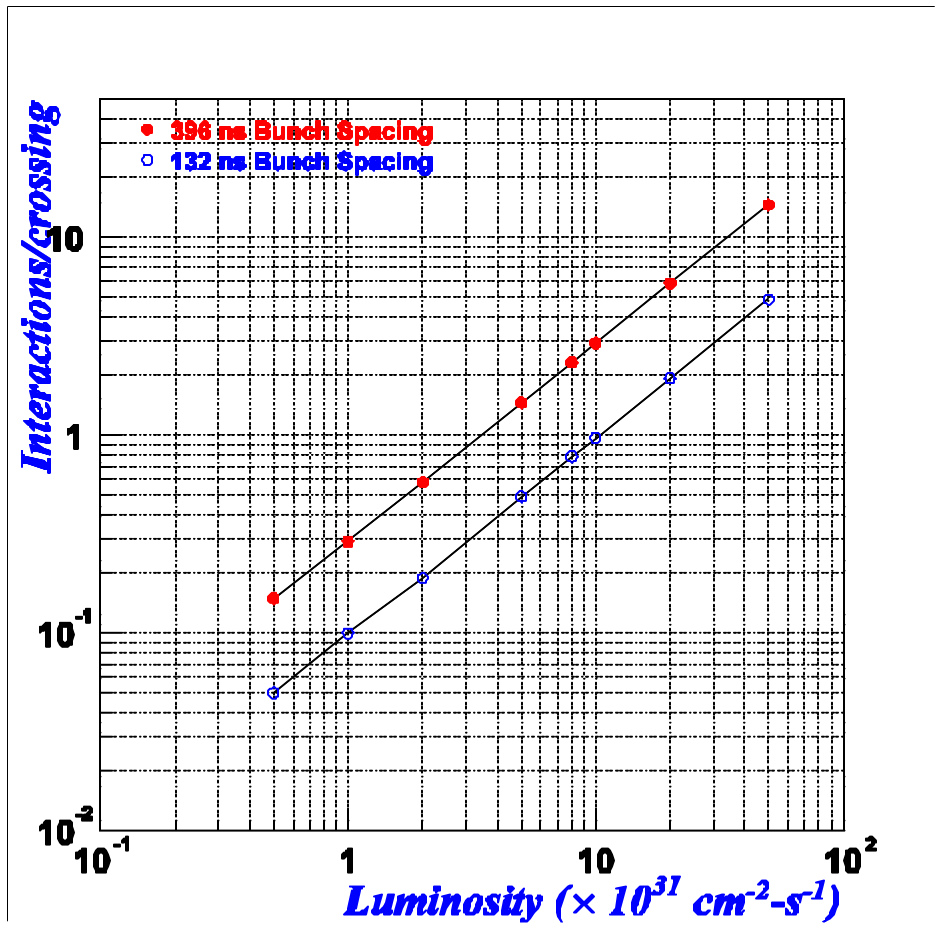
Track Finding Efficiency

- The curves on the right represent the probability that a charged track will fire a given Pt bin (or higher) as a function of the track Pt (measured by the offline software).
- The sharpness of the turn-on is related to the momentum resolution, and is consistent with 1.74%/GeV/c
- The plateau gives the overall efficiency: >95%



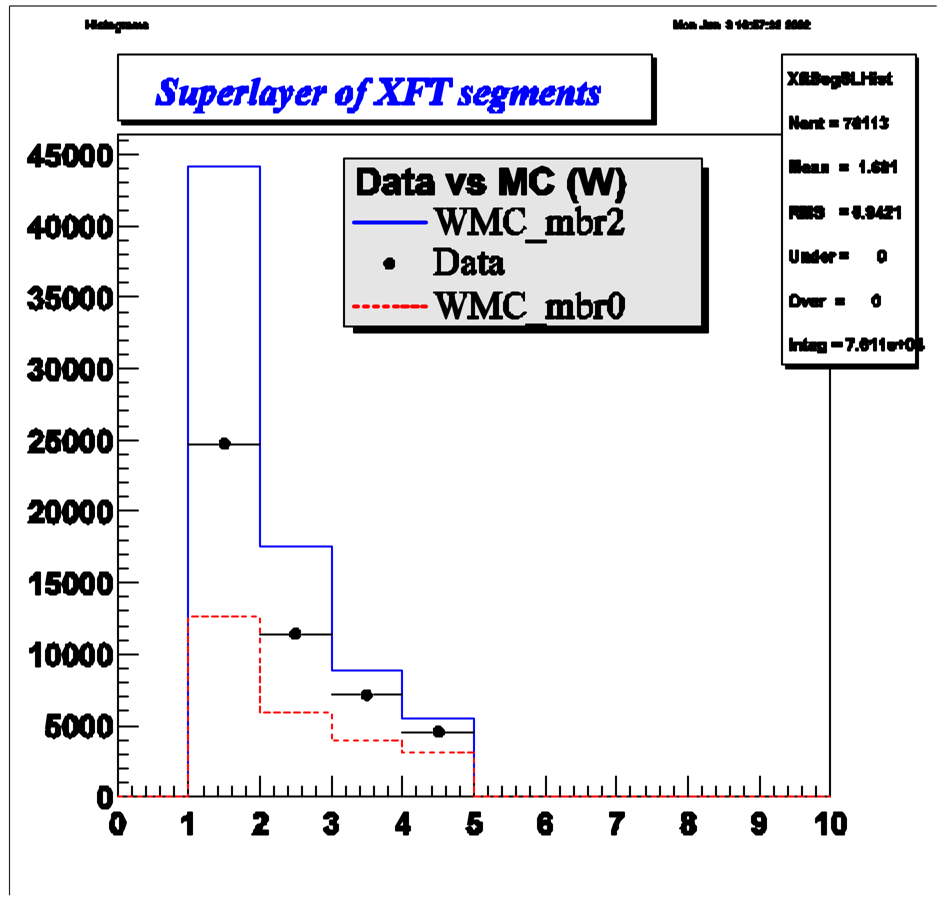
XFT Run IIb Upgrade

- The XFT was designed for a luminosity of:
  - $L=1x10^{32}cm^{-2}s^{-1}$ 396nsec bunch
    - <int/crossing> ~ 3
  - $L=2x10^{32}cm^{-2}s^{-1}$ 132nsec bunch
    - <int/crossing> ~ 2
- The Lab has stated that the
  - **"The Run IIb detectors should be designed to be efficient for the most important high-Pt physics processes at luminosities up to approximately $4x10^{32}$ cm^{-2} sec^{-1} at 396 nsec bunch spacing."**
  - Run IIb will operate at a factor of 4 above the XFT design luminosity



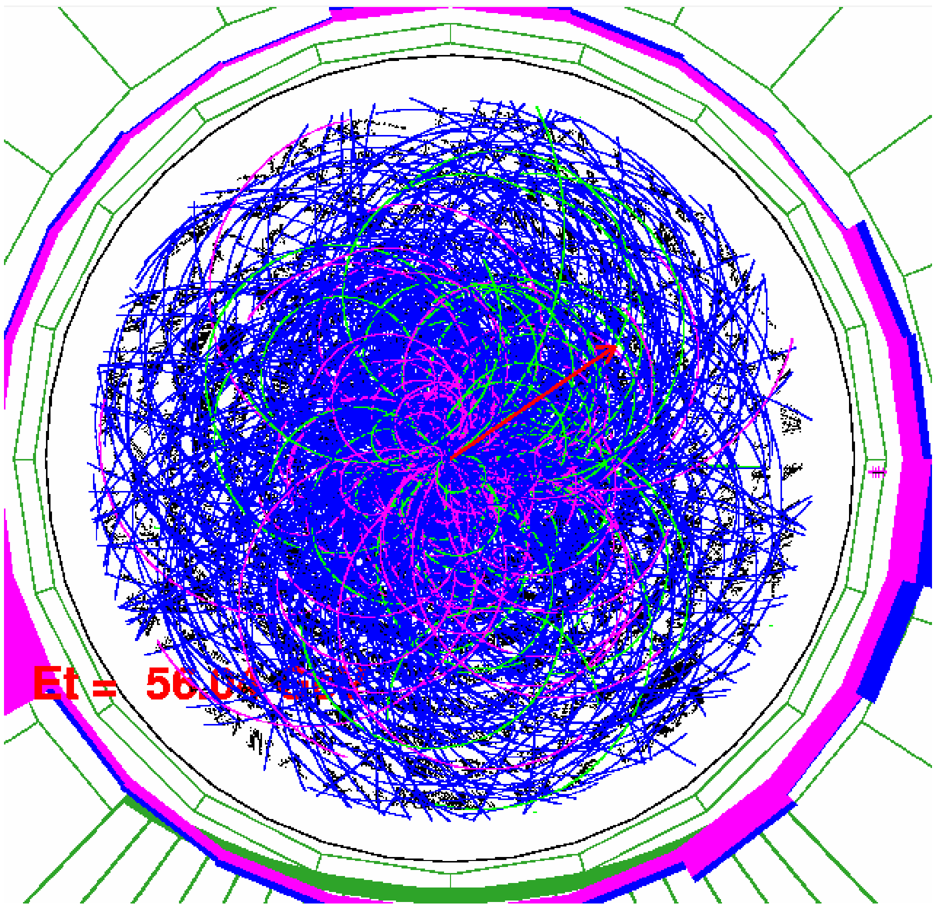
Occupancy Effects

- The occupancy in the COT is much higher than expected
- This combined with running at a lower number of required misses will lead to XFT degradation as the number of interactions increases.
- Running at at maximum of 10 <int/crossing> leads to much worse performance

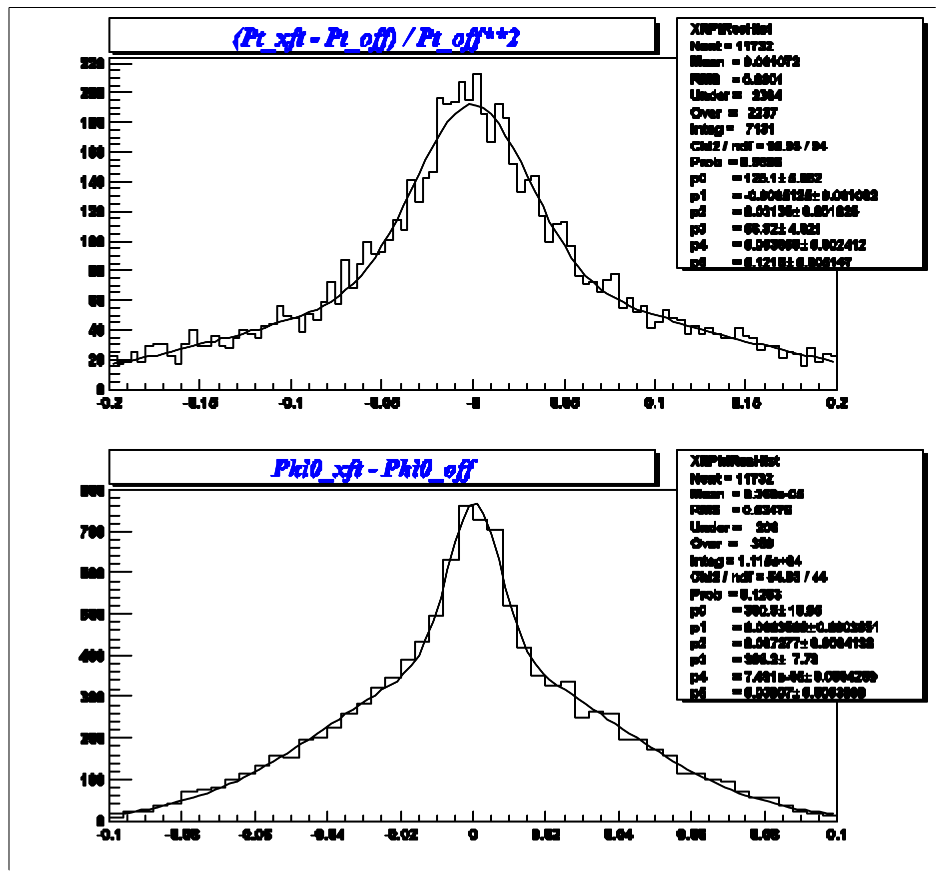


Extrapolated Performance

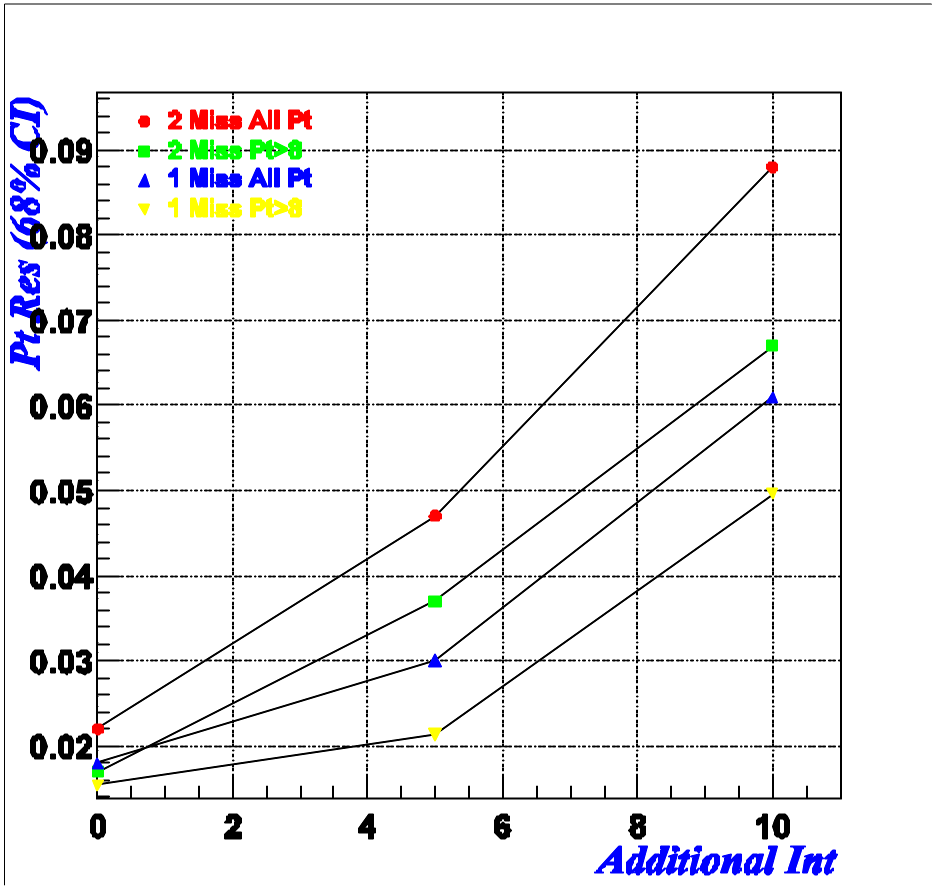
A ttbar event with 10 overlaid minbias

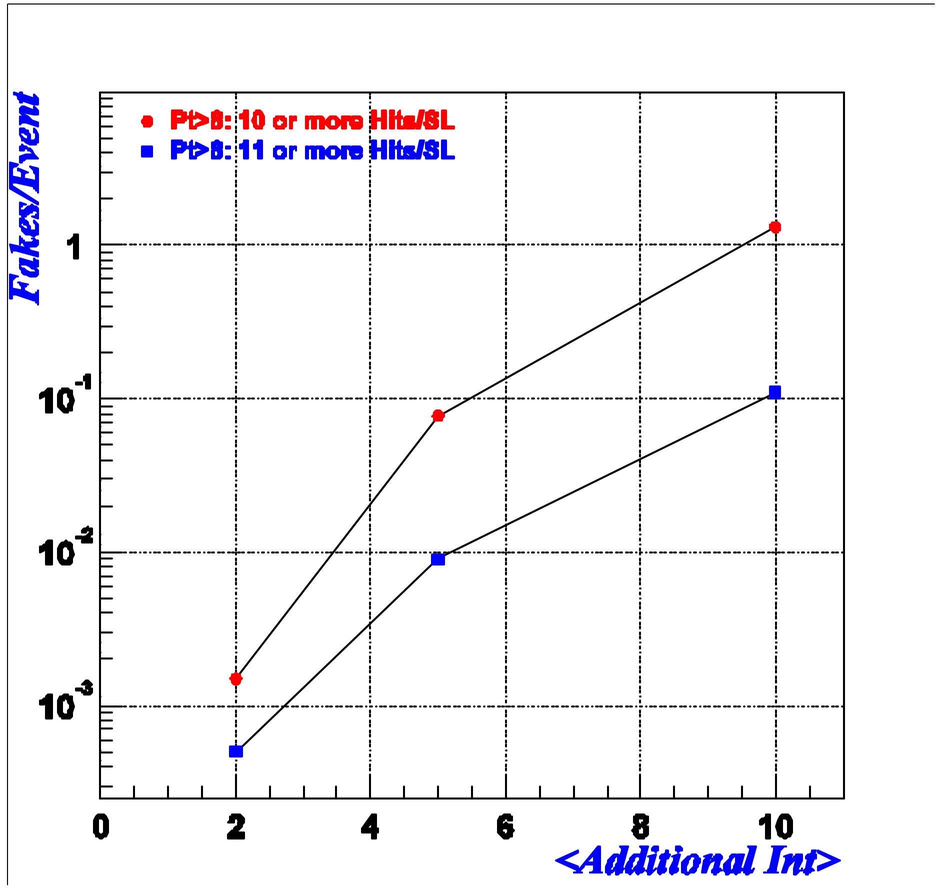


Phi and Pt resolution in 10 overlaid minbias



Performance at High Luminosity



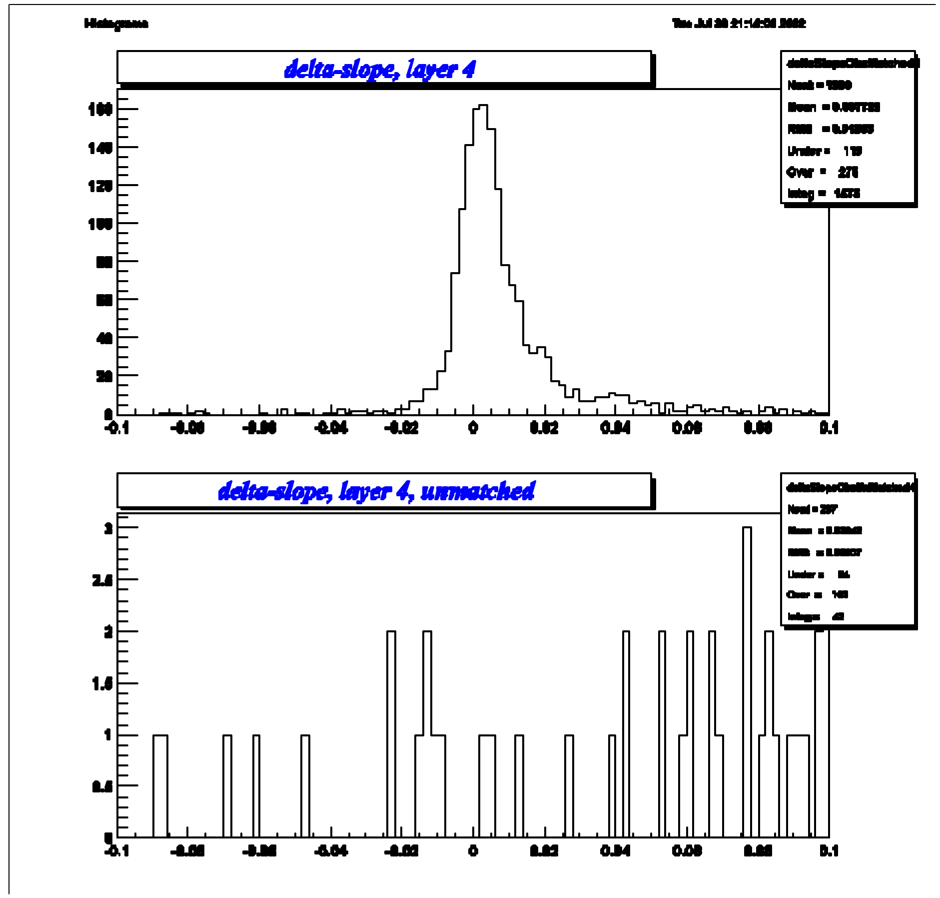


Improving The XFT

- Degradation of XFT occurs in 3 areas: momentum resolution, phi resolution, and fake tracks
- To improve things we need:
  - Better segment finding: This will reduce the number of spurious pixels reported to the Linker.
    - Axial Finders: improve phi and pt resolution.
    - Stereo Finders: Reject fake tracks
  - Better segment linking: Valid segments from different low pt tracks could be mistaken for a single high Pt track. This becomes a much bigger problem at high luminosity. Using better slope information at the linking stage reduces this problem.

Fake Tracks

- The plots show the difference in slope between found XFT tracks and the nearest true Monte Carlo track.
- The top plot is for “real” XFT tracks.
- The bottom plot is for “fake” (unmatched) XFT tracks.
- Conclusion: Fake tracks are due to combination of segments from ***different*** **real** tracks

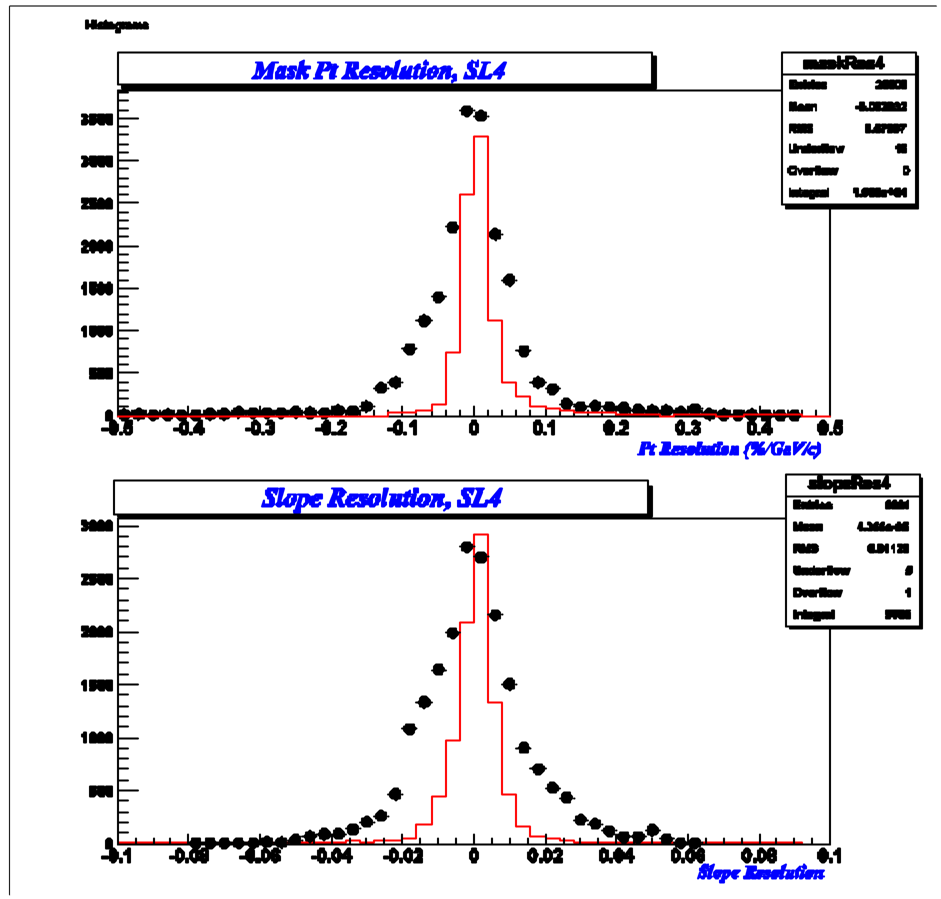


Algorithm Changes

- Hit Stage
  - Provide 6 times bins instead of the present 2
- Segment Finding Stage
  - Using 6 times bins, measure phi (pixel) position and slope at all 4 axial layers and 1 stereo layer.
  - Provide 5 slope bins at the outer two axial and outermost stereo layers, 3 slope bins at the inner two axial layers.
- Segment Linking Stage
  - Require matching slope and pixel at all 4 axial layers, instead of limited (low pt) slope requirement at the outer two layers.
  - Require stereo confirmation for high Pt tracks, stereo association for all tracks.

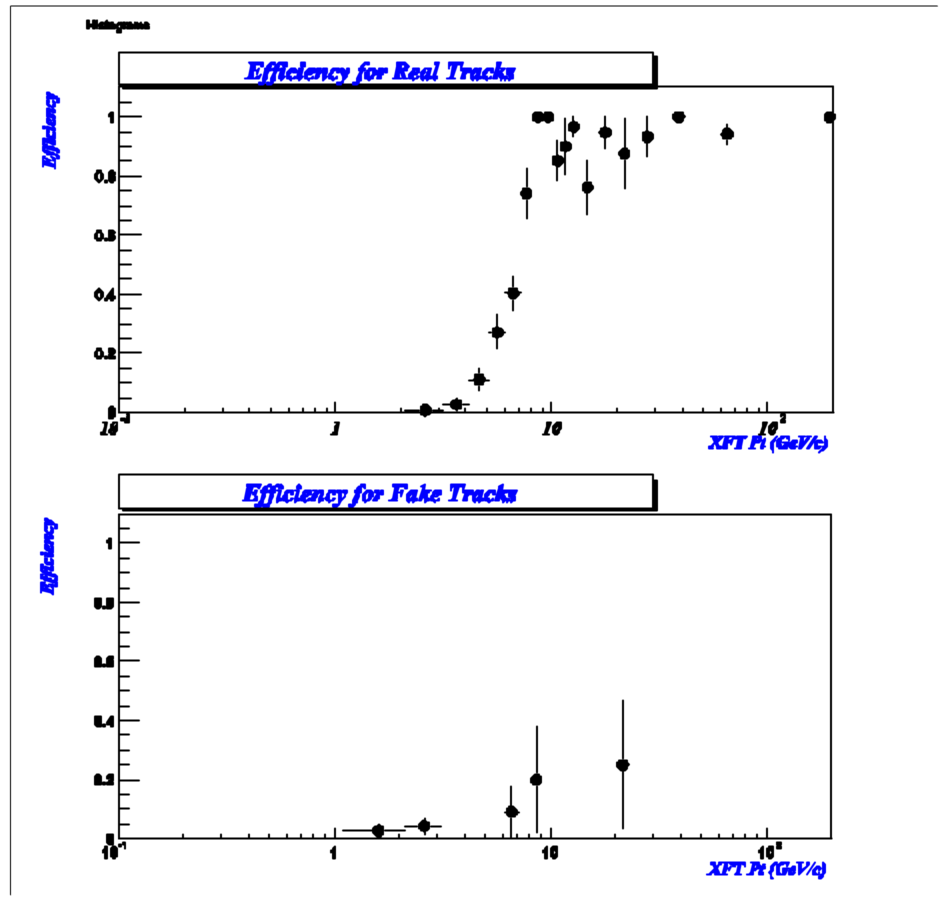
Impact of Additional Timing Information

- The additional resolution in timing at the hit level allows the Finder to measure the Pt or Slope of the segments with higfer precision.
- We have added this new timing info to our full XFT simulation, to understand the impact on resolution at the segment finding level.
- The top plot shows the improvement in slope resolution at the mask level. The solid curve uses the additional timing information.
- The bottom plot shows the same for the slope resolution at the mask level.



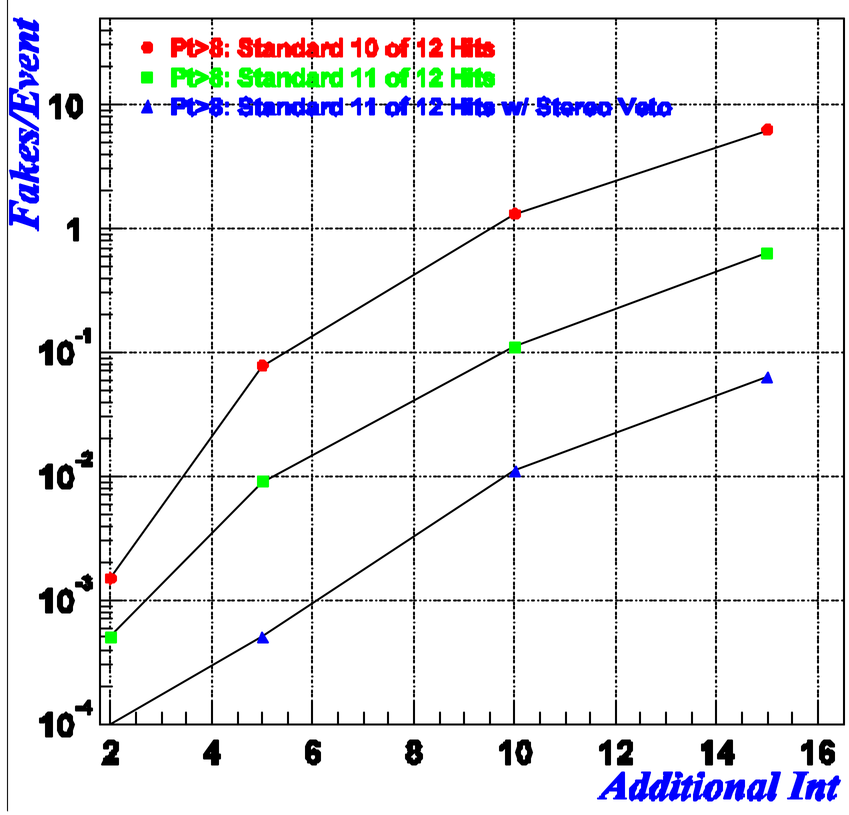
Impact on Segment Linking

- We have tested how better segment slope resolution can help reject fakes.
- In a Monte Carlo sample, we smear segments found by the expected slope resolution. We then ask if this “measured” slope is above a high Pt threshold.
- We require both segments from the outermost axial layer to have passed the high Pt threshold.
- The upper plot is the efficiency for true tracks to pass the threshold.
- The lower plot is the efficiency for fake tracks to pass the threshold.



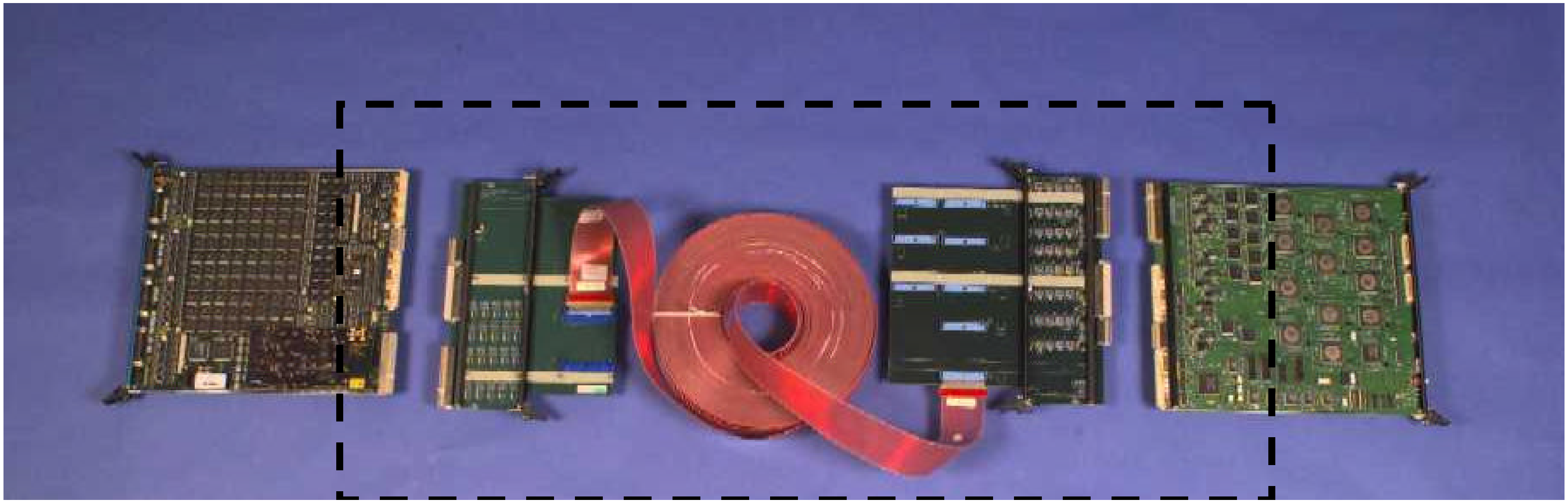
Impact of Stereo

- The stereo can have an impact in two ways:
  - Provide Z-pointing to tracks: Since EM and muon calorimeters are segmented in Z, coarse pointing can be very helpful in eliminating fakes
  - Confirmation Segment: Since often fake XFT tracks are the result of linking two unrelated low Pt segments, requiring another high Pt stereo segment in the allowed window around an axial track can be very powerful.
- Note that the stereo has no impact on phi/pt resolution.



TDC to Finder

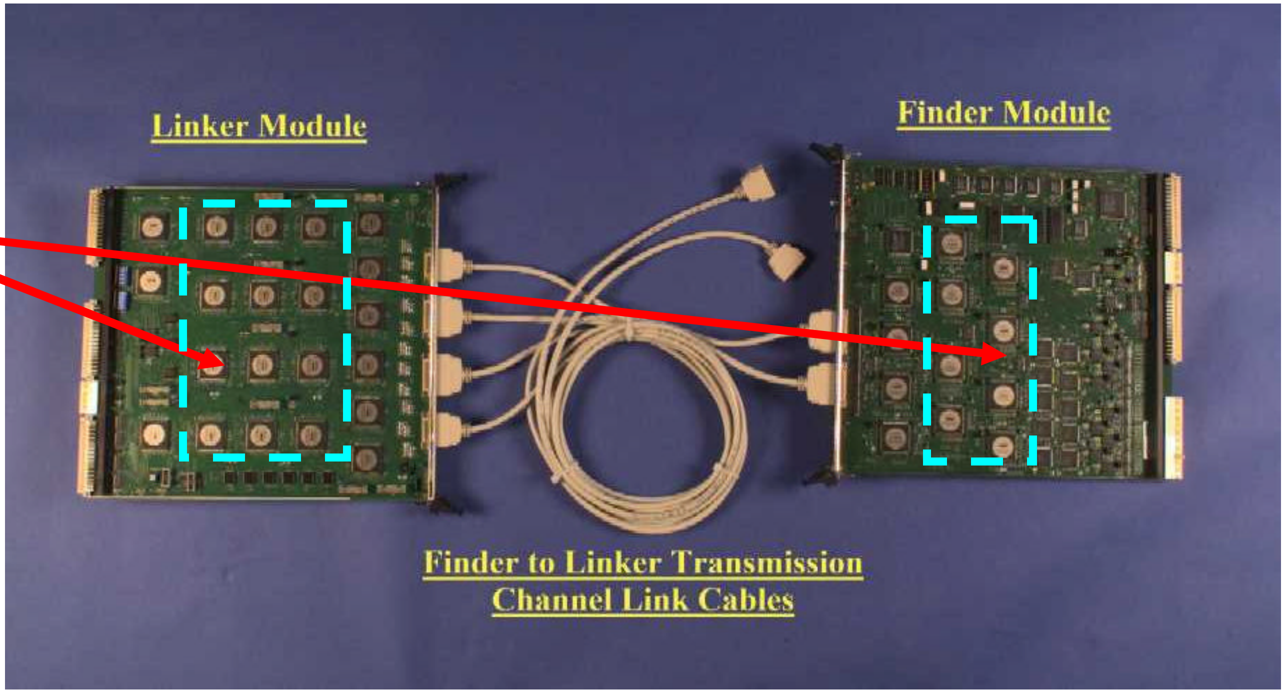
- The upgraded TDC replaces the current TDC + mezzanine card to provide hit information to the Finder.
- However, the TDC transition cards, cabling, and Finder transition cards in the present system are reused.
- Data is driven up the Ansley cables at the current clock of 22nsec. Two additional CDFCLK (@132nsec) are required to send up 6 time bins/wire versus the present 2 times bins/wire



Finder to Linker

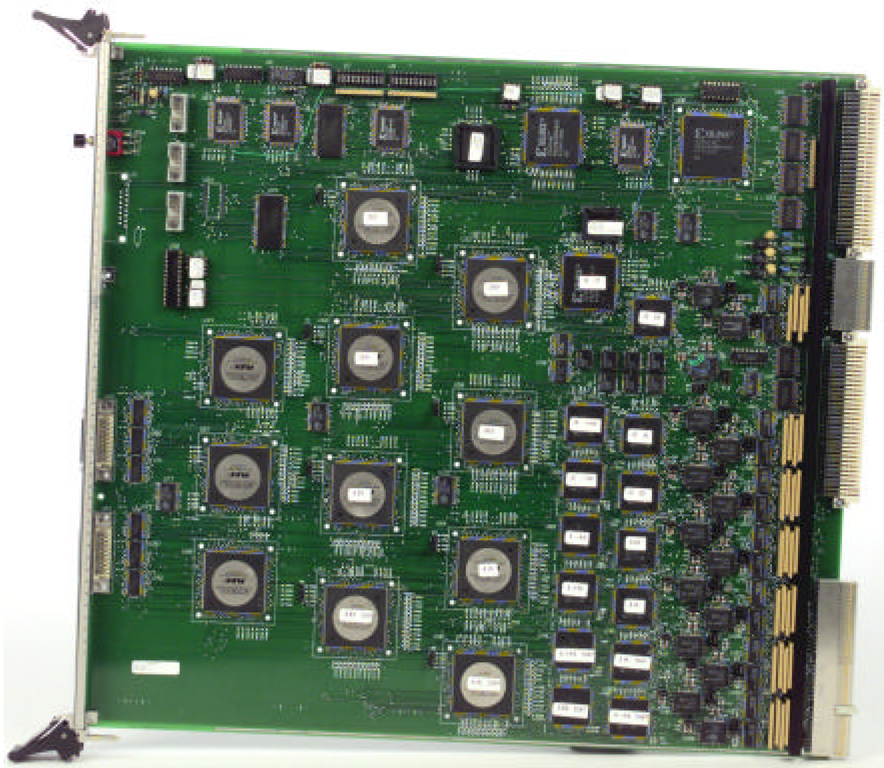
- The Finder control output, cabling, and Linker Input sections do not need to change. We use an additional 2 CDFCLKs (@132nsec) to transfer additional slope information.
- The Linker output section can also remain the same as the present system.

Algorithm chips need to be modified to handle increase in information.



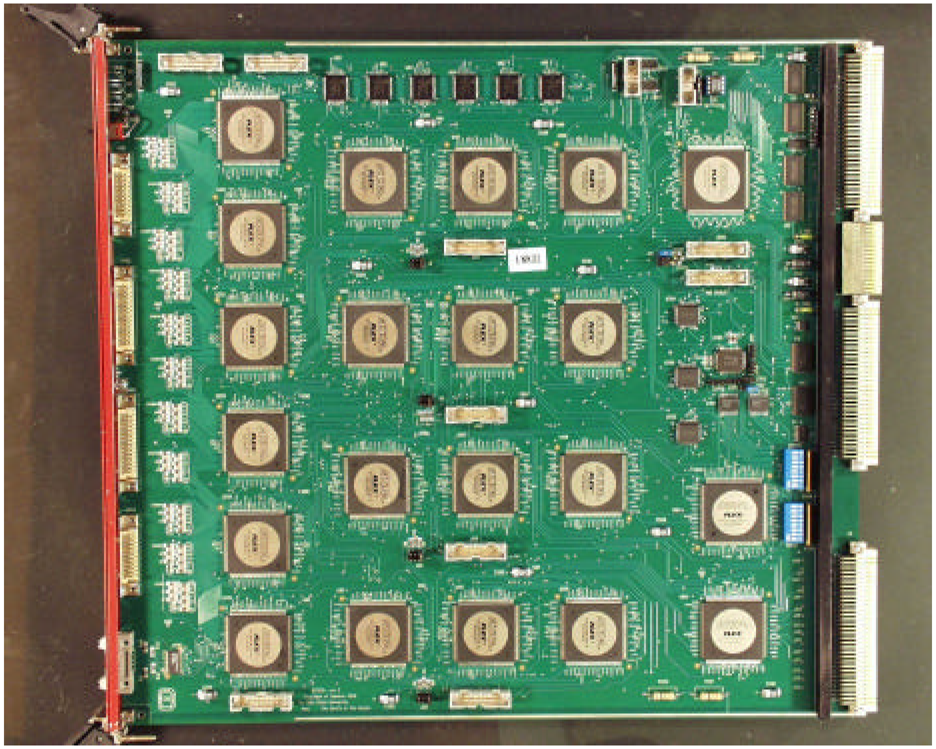
Finder Board

- The input capture section runs at the same speed and does not change.
- The pixel driver (output) section runs at the same speed and does not change.
- The primary change is to the Finder pattern recognition chips.
  - Need more masks
  - Need to run faster since time is taken to input more data (3x more hit data)
  - Target ALTERA Stratix EP1S20/25 as the replacement
- New board layout needed since BGA vs QFP



Linker Board

- The Input Formatter section runs at the same speed and does not change.
- The Output Formatter section runs at the same speed and does not change.
- The primary change is to the Finder pattern recognition chips.
  - Need more roads
  - Need to run faster since time is taken to input more data (more slope data)
  - Target ALTERA Stratix EP1S20/25 as the replacement
- New board layout needed since BGA vs QFP



Improving Pattern Recognition Chips

- New Finder Chips
  - **Expect factor of 7 more masks**
  - **Need to Run about factor of 2 faster (16nsec internal clock versus 33nsec internal clock)**

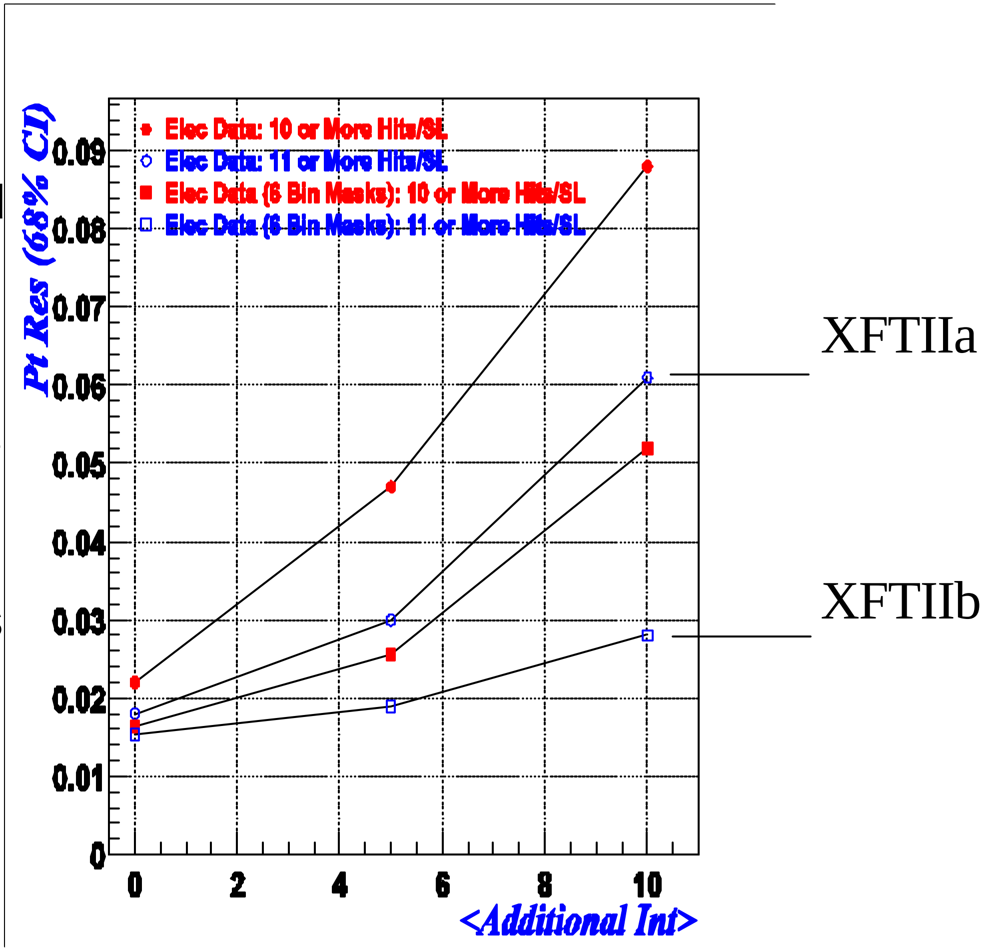
Chip	2 Time Bins, Masks	6 Time Bins, Masks
Finder Axial SL1	166	1344
Finder Axial SL2	227	1844
Finder Axial SL3	292	2056
Finder Axial SL4	345	2207

- **New Linker Chips**
  - **Expect factor of 3.3 more roads**
  - **Need to run about factor of 2 faster(16nsec internal clock versus 33nsec internal clock)**

Slope Bins	Roads
0,0,2,2	1200
3,3,5,5	4000

XFTIIb R&D

- Full simulation of RunIIb detector and occupancies necessary
  - Started on implementation of RunIIb XFT design using standard CDF environment
  - Preliminary indications of design performance
- Full simulation of new Linker chips using latest Altera FPGA design software tools
  - Factor of >10 more logic elements
  - Factor of >100 more memory
  - Advanced I/O features
    - LVDS, SERDES
  - Factor of 4-6 faster



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Target Implementation

- We have implemented the current Linker design in an Altera EP1S10 device, using the QUARTUS software package. Resources
  - 2404/10570 (22%) Logic Elements used
  - 3328/920,448 (<1%) memory bits used
- Timing simulation
  - CLK33 runs at a maximum of 7.5 nsec (old:25nsec)
  - CLK66 runs at a maximum of 10.8nsec (old:66nsec)

Chip	Current Implementation	Target Implementation
Finder Axial SL1	Altera Flex 10K50	Stratix EP1S20
Finder Axial SL2	Altera Flex 10K50	Stratix EP1S20
Finder Axial SL3	Altera Flex 10K50	Stratix EP1S20
Finder Axial SL4	Altera Flex 10K70	Stratix EP1S20
Linker	Altera Flex 10K50	Stratix EP1S20